TITLE OF THE INVENTION

SEMICONDUCTOR MEMORY DEVICE AND ITS MANUFACTURING METHOD

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is based upon and claims the benefit of priority from the prior Japanese Patent Application No. 2003-132703 filed May 12, 2003, the entire contents of which are incorporated herein by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a semiconductor memory device, e.g. a semiconductor memory device in which a memory cell includes a ferroelectric material.

2. Description of the Related Art

Ferroelectric memories are known in which a memory capacitor includes a ferroelectric material. Some of them are TC-parallel-unit series connection type ferroelectric memories. These memories have a structure in which a plurality of unit cells are electrically connected in series, the unit cell comprising a cell transistor (T) in which opposite ends of a capacitor (C) are connected between the source and drain of the transistor.

FIG. 21 is a sectional view schematically showing a TC-parallel-unit series connection type ferroelectric memory (hereinafter simply referred to as a

"semiconductor memory device" unless otherwise specified). As shown in FIG. 21, memory cell transistors 104 each composed of a gate electrode 102 and source/drain diffusion areas 103a, 103b are formed on a surface of a semiconductor substrate 101. A memory cell capacitor 114 composed of a lower electrode 111, a ferroelectric film 112, and an upper electrode 113 is formed above the transistor 104.

The lower electrode 111 is connected to the source/drain diffusion area 103a by a contact 121. The upper electrode 113 is connected to the source/drain diffusion area 103b via a connection layer 122, a plate electrode 123, and a contact 124. One of the memory cell transistors 104 is connected to a select transistor 131. A source/drain diffusion area 103a of the select transistor 131 is connected to a bit line 133 via a contact 132.

Further, the structure shown in FIG. 22 is known as a ferroelectric memory having a structure different from the TC-parallel-unit series connection type. In the ferroelectric memory of this structure, the source/drain diffusion area 103b shared by the two transistors 104 is connected to a bit line 133 via the contact 132. The upper electrode 113 and the plate electrode 123 constitute a single electrode extending in a direction perpendicular to the sheet of the drawing.

To reduce the size of a semiconductor memory device while increasing its density, it is desirable to reduce an area per unit cell. For the semiconductor memory devices shown in FIGS. 21 and 22, the area per unit cell has been reduced by scaling down a design rule.

Thus, the more the area per unit cell shrinks, the more the gate length of a transistor decreases. However, too small a gate length may result in a short channel effect. The short channel effect may cause the memory cell transistor to malfunction. Thus, with the structures shown in FIGS. 21 and 22, the reduction in the area per unit cell is limited.

Further, the more the area per unit cell shrinks, the higher the aspect ratios of the contacts 121, 124, and 132 become. With high aspect ratios, when the contact 121, 124, and 132 are formed, the corresponding contact holes may not be sufficiently filled with a conductive material. As a result, inappropriate contacts may occur. Further, it is difficult to form the contact holes themselves.

BRIEF SUMMARY OF THE INVENTION

According to a first aspect of the present invention, there is provided a semiconductor device comprising: a semiconductor substrate; a first trench formed in a surface of the semiconductor substrate and having a first side wall; a first impurity diffusion

area formed in the semiconductor substrate at a bottom of the first trench; a second impurity diffusion area formed in the surface of the semiconductor substrate, having one end in contact with the first side wall, and having the same conductive type as that of the first impurity diffusion area; a first gate electrode provided on the first side wall between the first impurity diffusion area and second impurity diffusion area with a gate insulating film interposed therebetween; a first lower electrode provided on the second impurity diffusion area; a first ferroelectric film provided on the first lower electrode; a first upper electrode provided on the first ferroelectric film; a first interconnection layer provided above the first upper electrode; and a first contact plug electrically connecting the first interconnection layer and first impurity diffusion area together.

According to a second aspect of the present invention, there is provided a semiconductor memory device having a plurality of memory cells connected in series, the memory cells each including a transistor and a capacitor having opposite ends connected to respective ends of the transistor, wherein each transistor comprises: a first impurity diffusion area formed in a semiconductor substrate at a bottom of one of a plurality of trenches formed in a surface of the semiconductor substrate; a second impurity diffusion

area formed in the surface of the semiconductor substrate between the trenches, having opposite ends contacting side walls of the trenches, and having the same conductive type as that of the first impurity diffusion area; and a gate electrode provided on the side wall of the trench between the first impurity diffusion area and the second impurity diffusion area with a gate insulating film interposed therebetween, and each capacitor comprises: a lower electrode provided on the second impurity diffusion area; a ferroelectric film provided on the lower electrode; and an upper electrode provided on the ferroelectric film.

According to a third aspect of the present invention, there is provided a method of manufacturing a semiconductor memory device comprising: forming a trench in a surface a semiconductor substrate; forming a first impurity diffusion area in the semiconductor substrate at a bottom of the trench; forming a gate insulating film on a side wall and the bottom of the trench; forming a gate electrode on the gate insulating film; forming a second impurity diffusion area in the surface of the semiconductor substrate, the second impurity diffusion area having one end contacting the side wall of the trench, the second impurity diffusion area having the same conductive type as that of the first impurity diffusion area; forming a lower electrode on the second impurity diffusion area;

forming a ferroelectric film on the lower electrode; forming an upper electrode on the ferroelectric film; forming a contact plug electrically connected to the first impurity diffusion area; and forming an interconnection layer above the upper electrode, the interconnection layer being electrically connected to the contact plug.

According to a fourth aspect of the present invention, there is provided a method of manufacturing a semiconductor memory device having a plurality of memory cells connected in series, the memory cells each including a transistor and a capacitor having opposite ends connected to respective ends of the transistor, the method comprising: forming a plurality of trenches in a surface of a semiconductor substrate, the trenches being apart from one another; forming first impurity diffusion areas in the semiconductor substrate at a bottom of each of the trenches; forming gate insulating films on side walls and a bottom of each of the trenches; forming gate electrodes on each of the gate insulating films; forming second impurity diffusion areas in the surface of the semiconductor substrate between the adjacent trenches, the second impurity diffusion areas each having opposite ends contacting the side walls of the trenches and having the same conductive type as that of the first impurity diffusion area; forming lower electrodes on each of the second

impurity diffusion areas; forming ferroelectric films on each of the respective lower electrodes, the ferroelectric films being apart from one another; forming upper electrodes on each of the respective ferroelectric films; forming contact plugs electrically connected to each of the first impurity diffusion areas; and forming interconnection layers above the respective upper electrodes, the interconnection layers each being electrically connected to each of the contact plugs.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING

FIG. 1 is a plan view schematically showing a part of a semiconductor memory device according to a first embodiment of the present invention;

FIG. 2 is a sectional view of FIG. 1;

FIG. 3 is a plan view schematically showing a manufacturing process for the semiconductor memory device in FIG. 1;

FIG. 4 is a sectional view of FIG. 3;

FIG. 5 is a sectional view schematically showing a step succeeding FIG. 4;

FIG. 6 is a sectional view schematically showing a step succeeding FIG. 5;

FIG. 7 is a sectional view schematically showing a step succeeding FIG. 6;

FIG. 8 is a sectional view of FIG. 7;

FIG. 9 is a sectional view schematically showing a

step succeeding FIG. 7;

FIG. 10 is a sectional view of FIG. 9;

FIG. 11 is a sectional view schematically showing a step succeeding FIG. 9;

FIG. 12 is a sectional view of FIG. 11;

FIG. 13 is a sectional view schematically showing a step succeeding FIG. 11;

FIG. 14 is a sectional view of FIG. 13;

FIG. 15 is a sectional view schematically showing a step succeeding FIG. 13;

FIG. 16 is a sectional view of FIG. 15;

FIG. 17 is a sectional view schematically showing a variation of a first embodiment;

FIG. 18 is a sectional view schematically showing a semiconductor memory device according to a second embodiment of the present invention;

FIG. 19 is a sectional view schematically showing a semiconductor memory device according to a third embodiment of the present invention;

FIG. 20 is a sectional view schematically showing a semiconductor memory device according to a fourth embodiment of the present invention; and

FIGS. 21 and 22 are sectional views schematically showing the conventional structure of a semiconductor memory device.

DETAILED DESCRIPTION OF THE INVENTION

Embodiments of the present invention will be

described below in detail with reference to the drawings. In the description below, components having substantially the same functions and arrangements are denoted by the same reference numerals. Duplicate description will be given only when required.

(First Embodiment)

A first embodiment relates to a ferroelectric memory having parallel-unit series connection type structure including cell transistors (T) and capacitors (C). FIG. 1 is a plan view schematically showing a part of a semiconductor memory device according to a first embodiment of the present invention. FIG. 2 is a sectional view taken along line II-II in FIG. 1.

As shown in FIGS. 1 and 2, an element separation insulating film 2 is formed on a surface of a semiconductor substrate composed of, for example, monocrystal silicon. The element separation insulating film 2 separates element areas from one another. The semiconductor memory device has a memory cell transistor (hereinafter simply referred to as a "transistor" unless otherwise specified) 3 (3a, 3b, and 3c), a memory cell capacitor (hereinafter simply referred to as a "capacitor") 4 (4a, 4b, and 4c), and a selection transistor 5. The transistor 3 and the capacitor 4 constitute a memory cell.

A plurality of trenches 6 is formed in a surface of the semiconductor substrate 1 in the respective

element areas. The transistor 3 is formed utilizing the semiconductor substrate 1 and the trenches 6. The transistor 3 (3a, 3b, and 3c) is composed of source/drain diffusion areas 11a and 11b and a gate insulating film 12, and a gate electrode 13.

The source/drain diffusion area 11a (impurity diffusion area) is formed in the semiconductor substrate 1 at the bottom of the trench 6. The source/drain diffusion area 11b (impurity diffusion area) is formed in the surface of the semiconductor substrate 1 between the trenches 6. The source/drain diffusion area 11b reaches a side wall of the trench 6. The source/drain diffusion area 11b is shared by the two transistors 3a and 3b in the trenches 6. The gate insulating film 12 is composed of, for example, a silicon oxide film and is formed along the side wall and bottom of the trench 6.

The gate electrode 13, composed of, for example, polysilicon, is formed on the gate insulating film 12 on the side wall of the trench 6 and on the opposite side walls of each trench 6. The gate electrode 13 is formed at least on the side wall of the trench 6 between the source/drain diffusion areas 11a and 11b. Thus, when a turn-on voltage from the transistor 3 is applied to the gate electrode 13, the source/drain diffusion areas 11a and 11b are electrically connected through a channel. The trench 6 is filled with an

insulating film 14 (second insulating film) such as a silicon oxide film.

The capacitor 4 is composed of a lower electrode 21, a ferroelectric film 22, and an upper electrode 23. The lower electrode 21 is composed of a material such as platinum (Pt), SRO ($SrRuO_3$), iridium (Ir), or iridium oxide (IrO_2), or a stacked film of these materials. The lower electrode 21 is formed on the surface of the semiconductor substrate 1 at a position corresponding to the source/drain diffusion area 11b. The lower electrode 21 is shared by the two capacitors 4a and 4b in the adjacent trenches 6.

The ferroelectric film 22 is formed for each capacitor 4. The ferroelectric films 22 belonging to the two capacitors 4a and 4b, respectively, are spaced from each other. The ferroelectric film 22 is composed of, for example, lead zirconate titanate (PZT). The upper electrode 23, composed of the same material as that of the lower electrode 21, is formed on the ferroelectric film 22.

A plate electrode (an interconnect layer) is provided on the upper electrode 23 via a connection layer 31 composed of a conductive material. The connection layer 31 is composed of, for example, aluminum (Al) or tungsten (W). The plate electrode 32 extends above the trench 6 and is connected to the connection layer 31 of the adjacent capacitor 4c beyond

the trench 6.

A contact 41 extends from almost the center of the lower end of the plate electrode 32 to penetrate the insulating film 14 between the gate electrodes 13 provided on the respective side walls of the trench 6. The gate insulating film 12 at the bottom of the trench 6 is partly removed. The contact 41 passes through this removed part to the source/drain diffusion area 11a. The contact 41 has a function of electrically connecting the plate electrode 32 and the source/drain diffusion area 11a together.

The selection transistor 5 is disposed so as to connect to a terminal one of the memory cells connected in series. The selection transistor 5 is configured similarly to the memory cell transistor 3. The source/drain diffusion area 11b of the selection transistor 5 is connected to a bit line 43 via a contact 42. Reference numeral 44 denotes an interlayer insulating film.

Now, with reference to FIGS. 3 to 16, description will be given of a manufacturing method for the semiconductor memory device configured as described above.

FIG. 3 is a plan view schematically showing a part of a manufacturing process for the semiconductor memory device in FIGS. 1 and 2. FIG. 4 is a sectional view taken along line IV-IV in FIG. 3, schematically showing

the structure of the semiconductor memory device. As shown in FIGS. 3 and 4, a protective film 7 composed of, for example, a silicon nitride film is formed on the surface of the semiconductor substrate 1. Then, a lithography process and an etching technique such as RIE (Reactive Ion Etching) are used to form a trench penetrating the protective film 7 and reaching the semiconductor substrate 1. Then, for example, a silicon oxide film is buried in the trench to form the element separation insulating film 2 having an STI (Shallow Trench Isolation) structure. Then, the lithography process and etching technique are used to form trenches 6 such as RIE (Reactive Ion Etching) are used to form the trenches 6 in the surface of the semiconductor substrate 1 in element areas AA.

Then, as shown in FIG. 5, an insulating film 12a constituting the gate insulating film 12 is formed on the inner wall of each trench 6 and on the surface of the semiconductor substrate 1 by, for example, thermal oxidation. Then, a conductive film 13a constituting the gate electrode 13 is deposited all over the surface of the semiconductor substrate 1 using an LPCVD (Low Pressure Chemical Vapor Deposition) method or the like. Next, a CMP (Chemical Mechanical Polish) method is used to flatten the conductive film 13a using the protective film 7 as a stopper. Then, etching such as RIE is carried out to etch back the conductive film 13a until

it has the same height as that of the surface of the semiconductor substrate 1. Next, the protective layer 7 is removed by etching.

Then, as shown in FIG. 6, the conductive film 13a and the insulating film 12a on the semiconductor substrate 1 are removed using, for example, the CMP method. As a result, the gate insulating film 12 is formed on the side wall of each trench 6. Further, the conductive film 13a is buried in the trench 6.

Then, as shown in FIG. 7 and FIG. 8 showing a cross section taken along line VIII-VIII in FIG. 7, a mask material (not shown) having a pattern of the gate electrodes 13 is deposited on the semiconductor substrate 1. Then, this mask is used to pattern the conductive film 13a by, for example, the RIE method. As a result, the gate electrodes 13 are formed. Subsequently, the mask material is removed.

Then, as shown in FIG. 9 and FIG. 10 showing a cross section taken along line X-X in FIG. 9, parts of the gate insulating film 12 on which no gate electrode is provided is removed using the lithography process and etching technique. As a result, the semiconductor substrate 1 is exposed from the bottoms of the trenches 6. Then, a mask material (not shown) is used to cover the entire semiconductor substrate 1 except for these exposed portions. Ions are then injected into the exposed portions to form the source/drain diffusion

area 11a. Subsequently, the mask material is removed.

Then, as shown in FIG. 11 and FIG. 12 showing a cross section taken along line XII-XII in FIG. 11, a material film for the insulating film 14 is deposited all over the surface of the semiconductor substrate 1 using the CVD method or the like. Next, parts of this material film which are located on the surface of the semiconductor substrate 1 are removed. As a result, the insulating film 14 is buried in the trenches 6.

Then, a mask material (not shown) is formed on the surface of the semiconductor substrate 1. The mask material has openings in areas in which the respective source/drain diffusion areas 11b are to be formed. Then, this mask material is used as a mask to inject ions to form the source/drain diffusion areas 11b. As a result, the transistor 3 (3a to 3c) and the selection transistor 5 are formed. Subsequently, the mask material is removed.

Then, as shown in FIG. 13 and FIG. 14 showing a cross section taken along line XIV-XIV in FIG. 13, the capacitor 4 (4a to 4c) is formed using the sputtering, lithography process, etching technique, and the like.

Then, as shown in FIG. 15 and FIG. 16 showing a cross section taken along line XVI-XVI in FIG. 15, an interlayer insulating film 44a is deposited all over the surface of the semiconductor substrate 1 using the CVD method or the like. Next, the lithographic

process, etching technique, and the like are used to form contact holes and interconnection trenches. Then, a conductive material is buried in the contact holes and interconnection trenches. The excessive conductive material on the interlayer insulating film 44a is removed using the CMP method or the like. As a result, the connection layers 31, the contacts 41, and the plate electrodes 32 are formed.

Then, as shown in FIGS. 1 and 2, a further interlayer insulating film 44 is formed all over the surface of the semiconductor substrate 1. Then, the lithographic process, etching technique, and the like are used to form contact holes penetrating the interlayer insulating film 44 and reaching the source/drain diffusion areas 11b, while forming interconnection trenches in the interlayer insulating film 44. Next, the excessive conductive material on the interlayer insulating film is removed. As a result, the contacts 42 and the bit lines 43 are formed.

In the semiconductor memory device according to the first embodiment of the present invention, the transistor 3 is formed using the trench 6 formed in the surface of the semiconductor substrate 1. The gate electrode 13 is disposed along the side wall of the trench 6. Thus, a gate length can be set regardless of the plain area of the transistor 3. Consequently, a

semiconductor memory device can be provided which can avoid causing the transistor 3 to produce a short channel effect even if the plain area of the transistor 3 decreases owing to the reduced size of the semiconductor memory device.

Further, the lower electrode 21 is connected to the source/drain diffusion area 11b without using any contacts (corresponding to the contacts 121 in FIG. 21). This reduces the distance between the surface of he semiconductor substrate 1 and the bit line 43, thus enabling a reduction in the aspect ratio of the contact 42. It can therefore reduce the possibility of defects in the contacts 42.

Further, in FIG. 21, it is impossible to sharply reduce the thickness of the interlayer insulating film between the gate electrode 102 and the lower electrode 111 for reliability and other reasons. Thus, since the film thickness of this portion must be maintained, the height of the contact 124 cannot be reduced. In contrast, in the semiconductor memory device according to the first embodiment, it is unnecessary to maintain the thickness of the interlayer insulating film, which is required for the structure in FIG. 21. Consequently, the aspect ratio of the contact 41 can be reduced. A shallower trench 6 enables the aspect ratio of the contact 41 to be further reduced. However, the shallower trench 6 reduces the gate length, so that too

shallow a trench 6 must be avoided. Thus, if the depth of the trench 6 is set so as to obtain a gate length that is, for example, as large as that in FIG. 21, then the aspect ratio of the contact 41 can be made somewhat smaller than that of the contact 124.

As a variation of the first embodiment, the gate electrode 13 can be formed in a manner different from the one described above. This method will be described below with reference to FIG. 17.

FIG. 17 schematically shows a step succeeding FIG. 4. As shown in FIG. 17, after the insulating film 12a has been formed, the CVD method, sputtering, and the like are used to deposit the conductive film 13a on the inner walls of the trenches 6 and on the surface of the semiconductor substrate 1. In this case, the conductive film 13a is as thick as or thicker than the gate electrode 13. Subsequently, the lithography process and etching technique are used to remove the conductive film 13a from the bottoms of the trenches 6 and from the surface of the semiconductor substrate 1. As a result, as shown in FIG. 8, the gate electrodes 13 are formed. Such a step also enables the formation of the same structure as that shown in FIGS. 1 and 2. Further, such a forming method for the gate electrodes 13 is applicable to a second to fourth embodiments, described below.

(Second Embodiment)

A second embodiment has not only the arrangements of the first embodiment but also an arrangement in which each gate electrode 13 is covered with an insulating film.

FIG. 18 is a sectional view schematically showing a semiconductor memory device according to a second embodiment of the present invention. As shown in FIG. 18, each gate electrode 13 is covered with a covering insulating film 51. The covering insulating film 51 is substantially composed of a material different from that of the insulating film 14, buried in the trench 6. More specifically, this material has an etching rate different from that of the insulating film 14. Further specifically, if the insulating film 14 is made of silicon oxide, the covering insulating film is made of silicon nitride.

The structure shown in FIG. 18 is realized by, for example, after the step in FIG. 8 for the first embodiment, depositing a material film for the covering insulating film 51 all over the surface of the semiconductor substrate 1 and patterning this material film using a known method.

According to the second embodiment of the present invention, the semiconductor memory device has a structure similar to that of the first embodiment and produces effects similar to those of the first

embodiment. Furthermore, in the second embodiment, the gate electrode 13 is covered with the covering insulating film 51. Thus, if a mask material is misaligned when a contact hole for the contact 41 is formed, it is avoidable that the contact 41 comes into contact with the gate electrode 13.

Further, the contact 41 can be formed in a self-alignment manner to the covering insulating film 51. When the contact 41 is formed in a self-alignment manner, it is not necessary to provide an additional margin for the possible misalignment of the mask. The area of the trench 6 can thus be reduced. As a result, the size of the semiconductor memory device can further be reduced.

(Third Embodiment)

A third embodiment relates to a general ferroelectric memory that does not have a TC-parallel-unit series connection type structure. That is, memory cells are each composed of a capacitor consisting of a ferroelectric material as well as a transistor, and are each arranged at the point of intersection between a word line and a bit line. The capacitors of the memory cells connected to the same word line are connected together via a plate line.

FIG. 19 is a sectional view schematically showing a semiconductor memory device according to a third embodiment of the present invention. As shown in

FIG. 19, only one end of each source/drain diffusion area 11b reaches the side wall of the corresponding trench 6. The ferroelectric film 22 and the upper electrode 23 both cover the lower electrode 21 from end to end. The upper electrode 23 is also used as the plate electrode 32.

The contact 42 is connected to the bit line 43 and penetrates the interlayer insulating film 44 and the insulating film 14 to reach the source/drain diffusion area 11a.

In the semiconductor memory device according to the third embodiment of the present invention, as in the case with the first embodiment, each transistor 3 is formed using the corresponding trench 6. Further, each gate electrode 13 is formed along the side wall of the corresponding trench 6. Thus, the gate length can be set regardless of the plain area of the transistor 3. Therefore, a semiconductor memory device can be provided which can avoid causing the transistor 3 to produce a short channel effect even if the plain area of the transistor 3 decreases owing to the reduced size of the semiconductor memory device.

(Fourth Embodiment)

A fourth embodiment has a structure corresponding to a combination of the third embodiment and the second embodiment. FIG. 20 is a sectional view schematically showing a semiconductor memory device according to a

fourth embodiment of the present invention. As shown in FIG. 20, each gate electrode 13 is covered with the covering insulating film 51. The other parts of the structure are similar to those of the third embodiment.

The semiconductor memory device according to the fourth embodiment of the present invention produces effects corresponding to the combination of the third embodiment and the second embodiment.

Additional advantages and modifications will readily occur to those skilled in the art. Therefore, the invention in its broader aspects is not limited to the specific details and representative embodiments shown and described herein. Accordingly, various modifications may be made without departing from the spirit or scope of the general inventive concept as defined by the appended claims and their equivalents.